Distributed by:

JAMECO® ELECTRONICS

www.Jameco.com ✦ 1-800-831-4242

The content and copyrights of the attached material are the property of its owner.

Jameco Part Number 43166

Rockwell

R65C02, R65C102 and R65C112 R65C00 Microprocessors (CPU)

DESCRIPTION

The 8-bit R65C00 microprocessor family of devices are produced using CMOS silicon gate technology which provides advanced system architecture for performance speed and system cost-effectiveness enhancements over their NMOS counterparts, the R6500 family of microprocessor devices.

Three CPU devices are available. All are software-compatible and provide 64K bytes of memory addressing, two interrupt inputs, and on-chip clock oscillators and/or drivers. All are bus-compatible with the NMOS R6500 family devices.

The CMOS family includes two microprocessors (R65C02 and R65C102) with on-board clock oscillators and drivers and one microprocessor (R65C112) driven by an external clock. The on-chip clock versions are aimed at high performance, low-cost applications where single phase inputs, crystal or RC inputs provide the time base. The slave processor version is geared for multiprocessor system applications where maximum timing control is mandatory. All R65C00 microprocessors are available in ceramic and plastic packaging, operating frequency of 1 MHz, 2 MHz, 3 MHz and 4 MHz, and commercial and industrial temperature versions. All three devices are available in 40-pin DIP or 44-pin PLCC packages.

FEATURES

- CMOS silicon gate technology
- Low Power (4 mA/MHz)
- Software compatible with R6502
- Single 5V ±5% power supply requirements
- Eight-bit parallel processing
- Decimal and binary arithmetic
- True indexing capability
- Programmable stack pointer
- Interrupt capability
- Non-maskable interrupt
- Eight-bit bidirectional data bus
- Memory address range of up to 64K bytes
- "Ready" input
- Direct memory access (DMA) capability
- Memory lock output
- 1 MHz, 2 MHz, 3 MHz, and 4 MHz versions
- Choice of external or on-chip clocks
- On-chip clock options
  —External single clock input
  —Direct crystal input (÷4)
- Commercial and industrial temperature versions
- Pipeline architecture
- Slave processor version (R65C112)

MAJOR FEATURES AND DIFFERENCES

Feature	R65C02	R65C102	R65C112
Pin compatible with NMOS R6502	X		
64K addressable bytes of memory	X	X	X
$\overline{IRQ}$ interrupt	X	X	X
On-chip clock oscillator		X	
External clock only	X		X
TTL level single phase clock input	X	X	
RC time base clock input	X	X	
Crystal time base clock input	X	X	
Single phase clock input			X
Two phase output clock	X	X	
SYNC and RDY signals	X	X	X
Bus Enable (BE) signal		X	X
Memory Lock ($\overline{ML}$) output signal		X	X
Direct Memory Access (DMA) capacity		X	X
$\overline{NMI}$ interrupt signal	X	X	X

ORDERING INFORMATION

Part Number:

R65C02 _ _ _
R65C102 _ _ _
R65C112

- Temp. Range (T_L to T_H)
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
  - M = −55°C to 125°C
- Frequency Range
  - 1 = 1 MHz
  - 2 = 2 MHz
  - 3 = 3 MHz
  - 4 = 4 MHz
- Package
  - C = 40-Pin Ceramic DIP
  - P = 40-Pin Plastic DIP
  - J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

This Material Copyrighted By Its Respective Manufacturer

INTERFACE SIGNALS

Figure 1 shows the pin assignments for the members of the R65C00 CPU family. All devices are housed in 40-pin ceramic or plastic dual-in-line (DIP) or 44-pin plastic leaded chip carrier (PLCC) packages.

Refer to the timing diagrams (Figures 3, 4, and 5) for the particular device in the following discussion.

CLOCK SIGNALS (R65C02)

The R65C02 requires an external Ø0 clock. See Figure 6 for an example clock circuit. Ø0 is a TTL level input that is used to generate the internal clocks of the R65C02. Two full level output clocks are generated by the R65C02. The Ø2 clock is in phase with Ø0. The Ø1 clock output is 180° out of phase with Ø0. When the input clock is stopped, the CPU is in the standby mode. See Figure 8 for special standby mode considerations.

For non-critical timing configurations, a simple RC or crystal network may be strapped between Ø0 (IN) and Ø1 (OUT).

CLOCK SIGNALS (R65C102)

The R65C102 internal clocks may be generated by a TTL level single phase input, an RC time base input, or a crystal time base input (÷ 4) using the XTLO and XTLI input pins. See Figure 7 for an example of a crystal time base circuit. Two full level output clocks are generated by the R65C102. The Ø2 clock output provides timing for external R/$\overline{W}$ operations. Addresses are valid after the address delay time (t_{ADS}) referenced to the falling edge of Ø2 (OUT). The Ø4 output is a quadrature output clock that is delayed from the falling edge of the Ø2 clock by delay time t_{AVS}. Using the Ø4 clock, addresses are valid at the rising edge of Ø4.

CLOCK SIGNALS (R65C112)

All internal clock signals for the R65C112 are generated by the input clock signal Ø2 (IN). Since this device is intended to be operated in the slave mode it does not have internal clock generation, but rather requires the external clock Ø2 (IN) from a host device. Figure 7 shows an example of a clock circuit for the R65C112 configured for slave mode.

ADDRESS BUS (A0–A15)

Address lines A0–A15 form a 16-bit address bus for memory and I/O exchanges on the data bus. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130 pF.

DATA BUS (D0–D7)

The data lines (D0–D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are tri-state buffers capable of driving one TTL load and 130 pF.

BUS ENABLE (BE)

This signal allows external control of the data and the address output buffers and R/$\overline{W}$. For normal operation, BE is high causing the address buffers and R/$\overline{W}$ to be active and the data buffers to be active during a write cycle. For external control, BE is held low to disable the buffers. BE is an asynchronous signal and therefore not related to, or controlled by the CPU internal clock signals. Figure 5 shows timing relationships of BE to R/$\overline{W}$ and address output buffers.

INTERRUPT REQUEST ($\overline{IRQ}$)

This TTL compatible input requests that an interrupt sequence begin within the microprocessor. $\overline{IRQ}$ is sampled at the falling edge of Ø2 prior to the last cycle of the instruction; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during Ø1. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further $\overline{IRQ}$s may occur. At the end of this cycle, the program counter low byte will be loaded from address FFFE, and program counter high byte from location FFFF, thus transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire OR operation.

MEMORY LOCK ($\overline{ML}$)

In a multiprocessor system, the $\overline{ML}$ output indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, RMB, SMB, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

NON-MASKABLE INTERRUPT ($\overline{NMI}$)

A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The $\overline{NMI}$ is sampled during Ø2; the current instruction is completed and the interrupt sequence begins during Ø1. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine.

NOTE

Since this interrupt is non-maskable, another $\overline{NMI}$ can occur before the first is finished. Care should be taken when using $\overline{NMI}$ to avoid this.

READY (RDY)

This input allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state, during or coincident with Ø2, will halt the microprocessor with the output address lines reflecting the current address. This condition will remain through a subsequent Ø2 in which the RDY signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

READ/WRITE (R/$\overline{W}$)

This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location.

SET OVERFLOW ($\overline{SO}$)

A negative transition on this line sets the overflow bit (V) in the processor status register. The signal is sampled prior to the rising edge of Ø2 by the $\overline{SO}$ setup time (t_{SOS}).

This Material Copyrighted By Its Respective Manufacturer

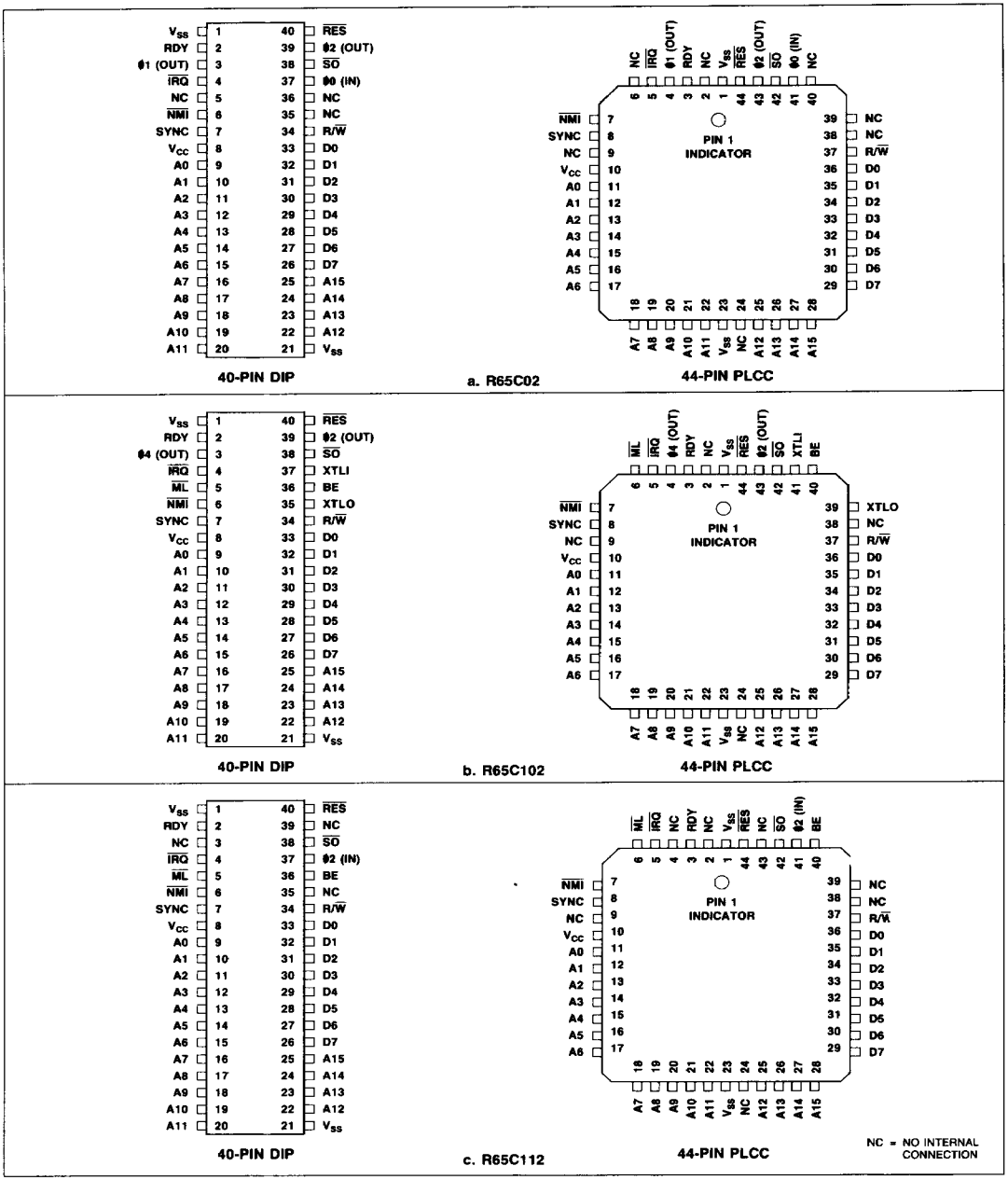


Figure 1. Pin Assignments

This Material Copyrighted By Its Respective Manufacturer

RESET ($\overline{RES}$)

This input resets the microprocessor. Reset must be held low for at least two clock cycles after V_{CC} reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles will cease microprocessing activity, followed by initialization after the positive edge on $\overline{RES}$.

When a positive edge is detected, there is an initialization sequence lasting seven clock cycles. Then the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.

SYNCHRONIZE (SYNC)

This output line identifies those cycles during which the microprocessor is fetching the instruction operation code (OP CODE). The SYNC line goes high during Ø1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the clock cycle in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

FUNCTIONAL DESCRIPTION

Figure 2 shows the block diagram of the R65C00 CPU internal architecture for all three devices. With the exception of the crystal oscillator, clock signals, Memory Lock (ML), and Bus Enable (BE) signals, the internal architecture of the three members of the R65C00 CPU of devices is identical. This block diagram supports the following text that describes the function of each of the device's major elements.

CRYSTAL OSCILLATOR (R65C102 Only)

The crystal oscillator, driven by a crystal across XTLO and XTLI, divides the crystal frequency by four to provide the basic Ø2 clock signal that drives the internal clock generator.

CLOCK GENERATOR

The clock generator develops all internal clock signals, and (where applicable) external clock signals, associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

INSTRUCTION REGISTER AND DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The R65C00 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

HARDWARE ENHANCEMENTS

The R65C00 family of CPU devices have incorporated hardware enhancements over their NMOS counterpart, the R6502. These hardware enhancements are:

- The NMOS device would ignore the assertion of a Ready (RDY) during a write operation. The CMOS family will stop the processor during Ø2 clock if RDY is asserted during a write operation.
- On the NMOS device, unused input-only pins ($\overline{IRQ}$, $\overline{NMI}$, RDY, $\overline{RES}$, and $\overline{SO}$) must be connected to a low impedance signal to avoid noise problems. These unused pins on the CMOS devices are internally connected by a high impedance to V_{CC} (approximately 250K ohms).

This Material Copyrighted By Its Respective Manufacturer

1

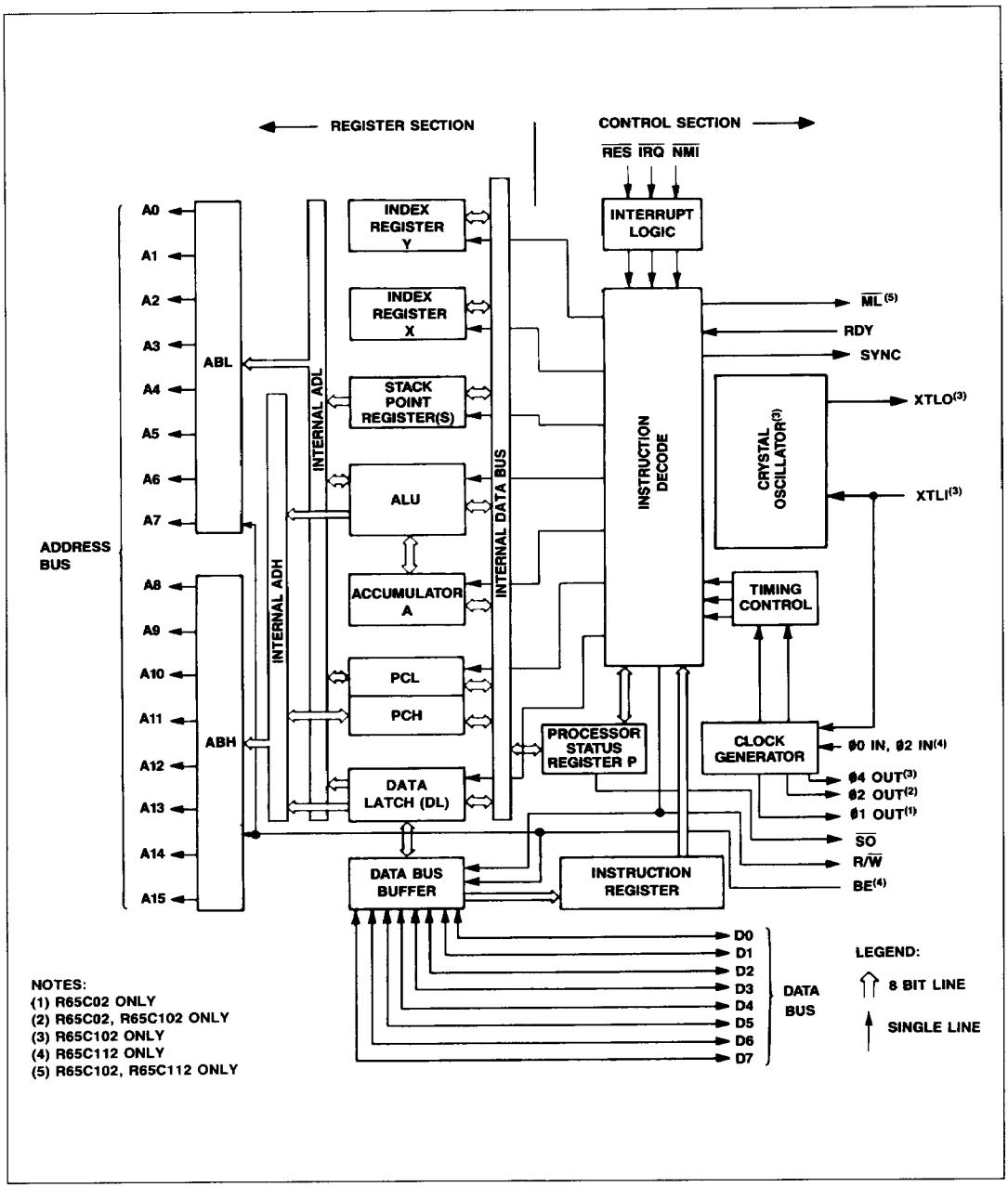


Figure 2. R65C00 Internal Architecture

This Material Copyrighted By Its Respective Manufacturer

ADDRESSING MODES

The R65C00 CPU family has 15 address modes (two more than the NMOS equivalent family). In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Op Code Matrix table (later in this product description) to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING [Accum] — This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING [IMM] — In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING [ABS] — In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING [ZP] — The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

ZERO PAGE INDEXED ADDRESSING [ZP, X or Y] — (X, Y indexing) — This form of addressing is used with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

ABSOLUTE INDEXED ADDRESSING [ABS, X or Y] — (X, Y indexing) — This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X" and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify fields, resulting in reduced coding and execution time.

INDEXED ABSOLUTE INDIRECT [(ABS, X)]* — The contents of the second and third instruction bytes are added to the X-register. The sixteen-bit result is a memory address containing the effective address. (JMP (ABS, X) only).

IMPLIED ADDRESSING [Implied] — In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING [Relative] — Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

ZERO PAGE RELATIVE ADDRESSING [ZP REL]* — This mode bit tests the zero page location specified for bit set/reset per the mask and performs a conditional relative branch based on the results of the bit test.

INDEXED INDIRECT ADDRESSING [(IND, X)] — In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents are the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING [(IND), Y] — In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT [(ABS)] — The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter. (JMP (ABS) only.)

INDIRECT [(IND)]* — The second byte of the instruction contains a zero page address serving as the indirect pointer.

ENHANCEMENTS OVER R6502

The CMOS family of microprocessor devices has been designed with many enhancements over the R6502 NMOS device while maintaining software compatibility. Besides the increased speed and lower power consumption inherent in CMOS technology, the R65C00 family has the following additional characteristics.

- 12 new instructions for a total of 68
- 59 new op codes, for a total of 210
- Two new addressing modes
- Seven software/operational enhancements
- Two hardware enhancements

*These addressing modes are not available to the NMOS CPU family (e.g., the R6502).

This Material Copyrighted By Its Respective Manufacturer

INSTRUCTION SET

Table 1 lists the instruction set for the CMOS CPU family in alphabetic order according to mnemonic. Tabe 2 lists the hexadecimal codes for each of the instructions that are new to the CMOS family and were not available in the NMOS R6502 device family. Table 3 lists those instructions that were available on the NMOS family, but have been assigned new addressing modes in the CMOS CPU family.

OPERATIONAL ENHANCEMENTS

Table 4 lists the operational enhancements that have been added to the CMOS family of CPU devices and compares the results with their NMOS R6502 counterpart.

Table 1. Alphabetic Listing of the R65C00 Instruction Set

	Mnemonic	Function		Mnemonic	Function
(2)	ADC	Add Memory to Accumulator with Carry		NOP	No Operation
(2)	AND	"AND" Memory with Accumulator			
	ASL	Shift Left One Bit (Memory or Accumulator)	(2)	ORA	"OR" Memory with Accumlator
(1)	BBR	Branch on Bit Reset		PHA	Push Accumulator on Stack
(1)	BBS	Branch on Bit Set		PHP	Push Processor Status on Stack
	BCC	Branch on Carry Clear	(1)	PHX	Push X Register on Stack
	BCS	Branch on Carry Set	(1)	PHY	Push Y Register on Stack
	BEQ	Branch on Result Zero		PLA	Pull Accumulator from Stack
(2)	BIT	Test Bits in Memory with Accumulator		PLP	Pull Processor Status from Stack
	BMI	Branch on Result Minus	(1)	PLX	Pull X Register from Stack
	BNE	Branch on Result not Zero	(1)	PLY	Pull Y Register from Stack
	BPL	Branch on Result Plus			
(1)	BRA	Branch Always	(1)	RMB	Reset Memory Bit
	BRK	Force Break		ROL	Rotate One Bit Left (Memory or Accumulator)
	BVC	Branch on Overflow Clear		ROR	Rotate One Bit Right (Memory or Accumulator)
	BVS	Branch on Overflow Set		RTI	Return from Interrupt
				RTS	Return from Subroutine
	CLC	Clear Carry Flag			
	CLD	Clear Decimal Mode		SBC	Subtract Memory from Accumulator with Borrow
	CLI	Clear Interrupt Disable Bit		SEC	Set Carry Flag
	CLV	Clear Overflow Flag		SED	Set Decimal Mode
(2)	CMP	Compare Memory and Accumulator		SEI	Set Interrupt Disable Status
	CPX	Compare Memory and Index X	(1)	SMB	Set Memory Bit
	CPY	Compare Memory and Index Y	(2)	STA	Store Accumulator in Memory
				STX	Store Index X in Memory
(2)	DEC	Decrement Memory by One		STY	Store Index Y in Memory
	DEX	Decrement Index X by One	(1)	STZ	Store Zero
	DEY	Decrement Index Y by One			
				TAX	Transfer Accumulator to Index X
(2)	EOR	"Exclusive-OR" Memory with Accumulator		TAY	Transfer Accumulator to Index Y
			(1)	TRB	Test and Reset Bits
(2)	INC	Increment Memory by One	(1)	TSB	Test and Set Bits
	INX	Increment Index X by One		TSX	Transfer Stack Pointer to Index X
	INY	Increment Index Y by One		TXA	Transfer Index X to Accumulator
				TXS	Transfer Index X to Stack Register
(2)	JMP	Jump to New Location		TYA	Transfer Index Y to Accumulator
	JSR	Jump to New Location Saving Return Address			
(2)	LDA	Load Accumulator with Memory			
	LDX	Load Index X with Memory			
	LDY	Load Index Y with Memory			
	LSR	Shift One Bit Right (Memory or Accumulator)			

Notes:
(1) Instruction not available on the NMOS family.
(2) R6502 instruction with additional addressing mode(s).

This Material Copyrighted By Its Respective Manufacturer

Table 2. Hexadecimal Codes For New Instructions in the R65C00 Microprocessors

Hex	Mnemonic	Description
80	BRA	Branch relative always [Relative]
DA	PHX	Push X on stack [Implied]
5A	PHY	Push Y on stack [Implied]
FA	PLX	Pull X from stack [Implied
7A	PLY	Pull Y from stack [Implied]
9C	STZ	Store zero [Absolute]
9E	STZ	Store zero [ABS, X]
64	STZ	Store zero [ZP]
74	STZ	Store zero [ZP, X]
1C	TRB	Test and reset memory bits with accumulator [ABS]
14	TRB	Test and reset memory bits with accumulator [ZP]
0C	TSB	Test and set memory bits with accumulator [ABS]
04	TSB	Test and set memory bits with accumulator [ZP]
0F-7F(1)	BBR	Branch on bit reset [Bit Manipulation, ZP, REL]
8F-FF(1)	BBS	Branch on bit set [Bit Manipulation, ZP, REL]
07-77(1)	RMB	Reset memory bit [Bit Manipulation, ZP]
87-F7(1)	SMB	Set memory bit [Bit Manipulation, ZP]

Note:
1. Most significant digit change only.

Table 3. Hexadecimal Codes For R65C00 Instructions With New Addressing Modes

Hex	Mnemonic	Description
72	ADC	Add memory to accumulator with carry [(IND)]
32	AND	AND memory with accumulator [(IND)]
3C	BIT	Test memory bits with accumulator [ABS, X]
34	BIT	Test memory bits with accumulator [ZP, X]
89	BIT	Test Immediate with accumulator [IMM]
D2	CMP	Compare memory and accumulator [(IND)]
3A	DEC	Decrement accumulator [Accum]
52	EOR	Exclusive Or memory with accumulator [(IND)]
1A	INC	Increment accumulator [Accum]
7C	JMP	Jump (New addressing mode) [(ABS, X)]
B2	LDA	Load accumulator with memory [(IND)]
12	ORA	OR memory with accumulator [(IND)]
F2	SBC	Subtract Memory from accumulator with borrow [(IND)]
92	STA	Store accumulator in memory [(IND)]

Table 4. R65C00 Operational Enhancements

Function	NMOS R6502 Microprocessor	CMOS R65C00 Family Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use).
Jump Indirect, operand = XXFF.	Page address does not increment.	Page address increments and adds one additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D = 0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flag adds one additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.

This Material Copyrighted By Its Respective Manufacturer

1

INSTRUCTION SET OP CODE MATRIX

The following matrix shows the 210 Op Codes associated with the R65C00 family of CPU devices. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode, the number of instruction bytes, and the number of machine cycles associated with each Op Code. Also, refer to the instruction set summary for additional information on these Op Codes.

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6			TSB ZP 2 5	ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2		TSB ABS 3 6	ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*	ORA (IND) 2 5		TRB ZP 2 5	ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*	INC Accum 1 2		TRB ABS 3 6	ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR ABS 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND), Y 2 5*	AND (IND) 2 5		BIT ZP, X 2 4	AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*	DEC Accum 1 2		BIT ABS, X 3 4*	AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*	EOR (IND) 2 5			EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*	PHY Implied 1 3			EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6†			STZ ZP 2 3	ADC ZP 2 3†	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2†	ROR Accum 1 2		JMP (ABS) 3 6	ADC ABS 3 4†	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND), Y 2 5*†	ADC (IND) 2 5†		STZ ZP, X 2 4	ADC ZP, X 2 4†	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*†	PLY Implied 1 4		JMP (ABS, X) 3 6	ADC ABS, X 3 4*†	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8	BRA Relative 2 3*	STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2	BIT IMM 2 2	TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND), Y 2 6	STA (IND) 2 5		STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2		STZ ABS 3 4	STA ABS, X 3 5	STZ ABS, X 3 5	BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*	LDA (IND) 2 5		LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*	CMP (IND) 2 5			CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*	PHX Implied 1 3			CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6†			CPX ZP 2 3	SBC ZP 2 3†	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2†	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4†	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*†	SBC (IND) 2 5†			SBC ZP, X 2 4†	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*†	PLX Implied 1 4			SBC ABS, X 3 4*†	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

— New Opcode

0

0 BRK Implied 1 7

—OP Code
—Addressing Mode
—Instruction Bytes; Machine Cycles

†Add 1 to N if in decimal mode.
*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
Add 2 to N if branch occurs to different page.

This Material Copyrighted By Its Respective Manufacturer

INSTRUCTION SET SUMMARY

MNEMONIC	OPERATION	IMMEDIATE OP	IMMEDIATE n	IMMEDIATE #	ABSOLUTE OP	ABSOLUTE n	ABSOLUTE #	ZERO PAGE OP	ZERO PAGE n	ZERO PAGE #	ZP REL OP	ZP REL n	ZP REL #	ACCUM. OP	ACCUM. n	ACCUM. #	IMPLIED OP	IMPLIED n	IMPLIED #	(IND, X) OP	(IND, X) n	(IND, X) #	(IND), Y OP	(IND), Y n	(IND), Y #	Z, PAGE, X OP	Z, PAGE, X n	Z, PAGE, X #	ABS, X OP	ABS, X n	ABS, X #	(ABS, X) OP	(ABS, X) n	(ABS, X) #	ABS, Y OP	ABS, Y n	ABS, Y #	RELATIVE OP	RELATIVE n	RELATIVE #	(IND) OP	(IND) n	(IND) #	Z, PAGE, Y OP	Z, PAGE, Y n	Z, PAGE, Y #	PROCESSOR STATUS CODES 7 N	6 V	5 ·	4 B	3 D	2 I	1 Z	0 C
ADC	A + M + C → A (1) (5) (7)	69	2	2	6D	4	3	65	3	2										61	6	2	71	5	2	75	4	2	7D	4	3				79	4	3				72	5	2				N	V					Z	C
AND	A · M → A (1)	29	2	2	2D	4	3	25	3	2										21	6	2	31	5	2	35	4	2	3D	4	3				39	4	3				32	5	2				N						Z	
ASL	C ← 7 0 ← 0				0E	6	3	06	5	2				0A	2	1										16	6	2	1E	7	3															N						Z	C
BBR (#0–7)	Branch on M# = 0										0F	5	3																																							
BBS (#0–7)	Branch on M# = 1										8F	5	3																																							
BCC	Branch on C = 0 (2)										FF																											90	2	2											
BCS	Branch on C = 1 (2)																																					B0	2	2											
BEQ	Branch on Z = 1 (2)																																					F0	2	2											
BIT	A ∧ M (6)	89	2	2	2C	4	3	24	3	2																34	4	2	3C	4	3															M7	M6					Z	
BMI	Branch on N = 1 (2)																																					30	2	2											
BNE	Branch on Z = 0 (2)																																					D0	2	2											
BPL	Branch on N = 0 (2)																																					10	2	2											
BRA	Branch Always (2)																																					80	2	2											
BRK	Break																00	7	1																													1					
BVC	Branch on V = 0 (2)																																					50	2	2											
BVS	Branch on V = 1 (2)																																					70	2	2											
CLC	0 → C																18	2	1																																0
CLD	0 → D																D8	2	1																																0	
CLI	0 → I																58	2	1																															0	
CLV	0 → V																B8	2	1																															0	
CMP	A – M	C9	2	2	CD	4	3	C5	3	2										C1	6	2	D1	5	2	D5	4	2	DD	4	3				D9	4	3				D2	5	2				N						Z	C
CPX	X – M	E0	2	2	EC	4	3	E4	3	2																																											
CPY	Y – M	C0	2	2	CC	4	3	C4	3	2																																											
DEC	M – 1 → M or A – 1 → A				CE	6	3	C6	5	2				3A	2	1										D6	6	2	DE	7	3															N						Z	
DEX	X – 1 → X																CA	2	1																																	
DEY	Y – 1 → Y																88	2	1																																	
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2										41	6	2	51	5	2	55	4	2	5D	4	3				59	4	3				52	5	2				N						Z	
INC	M + 1 → M or A + 1 → A				EE	6	3	E6	5	2				1A	2	1										F6	6	2	FE	7	3															N						Z	
INX	X + 1 → X																E8	2	1																																	
INY	Y + 1 → Y																C8	2	1																																	
JMP	Jump to New Loc (8)				4C	3	3																									7C	6	3																	
JSR	Jump Sub				20	6	3																																													
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2										A1	6	2	B1	5	2	B5	4	2	BD	4	3				B9	4	3				B2	5	2				N						Z	
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			B6	4	2				BE	4	3															
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2																B4	4	2																		N						Z	
LSR	0 → 7 C				4E	6	3	46	5	2				4A	2	1										56	6	2	5E	7	3															0						Z	C
NOP	No Operation																EA	2	1																																	
ORA	A ∨ M → A (1)	09	2	2	0D	4	3	05	3	2										01	6	2	11	5	2	15	4	2	1D	4	3				19	4	3				12	5	2				N						Z	
PHA	A → Ms S – 1 → S																48	3	1																																	
PHP	P → Ms S – 1 → S																08	3	1																																	
PHX	X → Ms S – 1 → S																DA	3	1																																	
PHY	Y → Ms S – 1 → S																5A	3	1																																	
PLA	S + 1 → S Ms → A																68	4	1																														N						Z	
PLP	S + 1 → S Ms → P																28	4	1																														(Restored)							
PLX	S + 1 → S Ms → X																FA	4	1																														N						Z	
PLY	S + 1 → S Ms → Y																7A	4	1																														N						Z	
RMB (#0–7)	Ø → M (4)																																																		
ROL	C ← 7 0 ← C				2E	6	3	26	5	2				2A	2	1										36	6	2	3E	7	3															N						Z	C
ROR	C → 7 0 → C				6E	6	3	66	5	2				6A	2	1										76	6	2	7E	7	3															N						Z	C
RTI	Return Int																40	6	1																														(Restored)							
RTS	Return Sub																60	6	1																																	
SBC	A – M – C → A (1) (3) (5)	E9	2	2	ED	4	3	E5	3	2										E1	6	2	F1	5	2	F5	4	2	FD	4	3				F9	4	3				F2	5	2				N	V					Z	C
SEC	1 → C																38	2	1																																	1
SED	1 → D																F8	2	1																																	1
SEI	1 → I																78	2	1																																	1
SMB (#0–7)	1 → M (4)																																																		
STA	A → M				8D	4	3	85	3	2										81	6	2	91	6	2	95	4	2	9D	5	3				99	5	3				92	5	2				N						Z	
STX	X → M				8E	4	3	86	3	2																96	4	2																		N						Z	
STY	Y → M				8C	4	3	84	3	2																																											
STZ	Ø → M				9C	4	3	64	3	2																74	4	2	9E	5	3															N						Z	
TAX	A → X																AA	2	1																																	
TAY	A → Y																A8	2	1																																	
TRB	A ∧ M → M	1C	6	3	14	5	2																																											
TSB	A ∨ M → M	0C	6	3	04	5	2																																											
TSX	S → X																BA	2	1																														N						Z	
TXA	X → A																8A	2	1																														N						Z	
TXS	X → S																9A	2	1																																	
TYA	Y → A																98	2	1																														N						Z	

Notes:

1. Add 1 to N if page boundary is crossed.
2. Add 1 to N if branch occurs to same page.
   Add 2 to N if branch occurs to different page.
3. Carry not (C) = Borrow.
4. Effects 8-bit data field of the specified zero page address.
5. Add 1 to N if in Decimal Mode.
6. On the Bit immediate instruction, the results of the M_7 and M_6 bits (N and V flags) are indeterminate and should be considered invalid.
7. If in Decimal Mode, Z flag is invalid. Accumulator must be checked for zero result.
8. JMP (OP Code 6C) is an Absolute Indirect Addressing Mode (ABS).

LEGEND

X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selected zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
+ = Add
- = Subtract
∧ = And
∨ = Or
⊻ = Exclusive or
n = Number of cycles
# = Number of Bytes

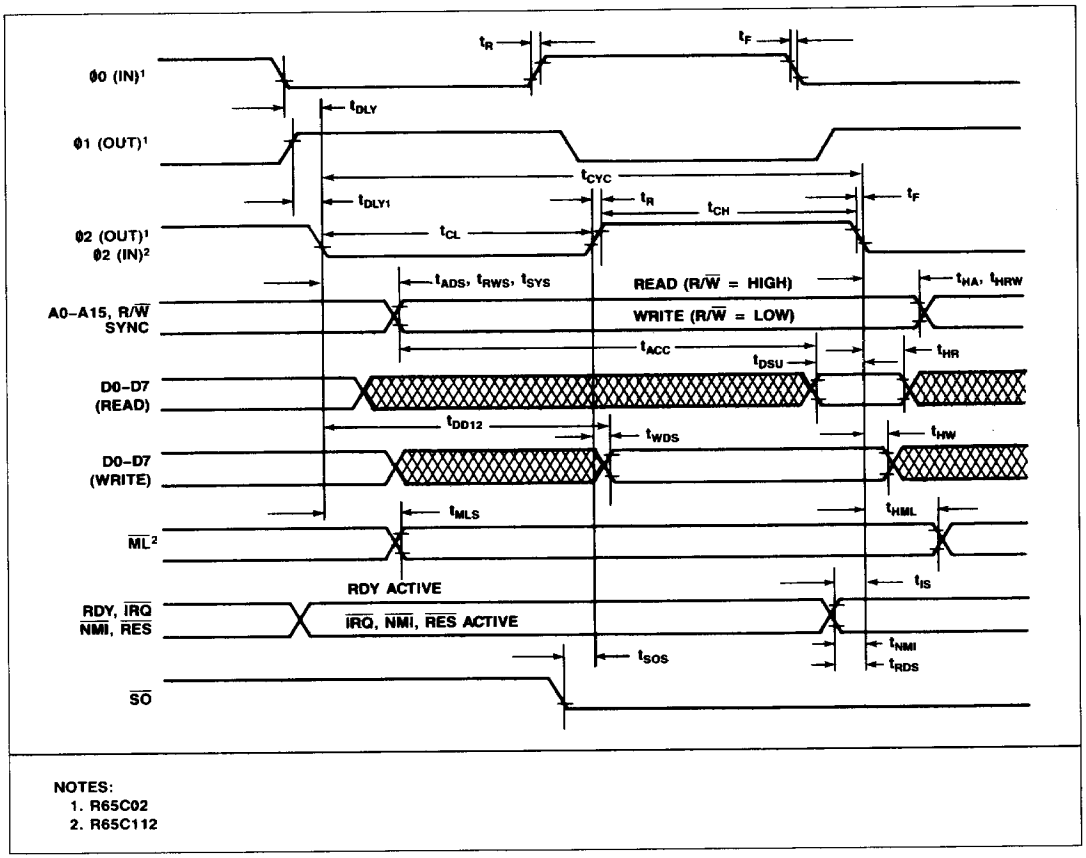
This Material Copyrighted By Its Respective Manufacturer

SWITCHING CHARACTERISTICS (Over operating conditions unless otherwise noted)

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
CLOCK TIMING										
Ø2 Cycle Time	t_{CYC}	1000	Note 1	500	Note 1	333	Note 1	250	Note 1	ns
Ø2 Low Pulse Width	t_{CL}	430	5000	210	5000	150	5000	100	5000	ns
Ø2 High Pulse Width	t_{CH}	450	—	220	—	160	—	110	—	ns
Ø0 Low to Ø2 Low Skew[2]	t_{DLY}	—	50	—	50	—	40	—	30	ns
Ø2 Low to Ø1 High Skew[2]	t_{DLY1}	-20	20	-20	20	-20	20	-20	20	ns
XTLI High to Ø2 Low[4]	t_{DXI}	—	100	—	100	—	100	—	100	ns
XTLO Low to Ø2 Low[4]	t_{DXO}	—	75	—	75	—	75	—	75	ns
Ø2 Low to Ø4 High Delay[4]	t_{AVS}	—	250	—	125	—	85	—	65	ns
Ø4 Low Pulse Width[4]	$t_{\phi 4L}$	430	—	210	—	150	—	100	—	ns
Ø4 High Pulse Width[4]	$t_{\phi 4H}$	450	5000	220	5000	160	5000	110	5000	ns
Clock Rise and Fall Times	t_R, t_F	—	25	—	20	—	15	—	12	ns
READ/WRITE TIMING										
R/$\overline{W}$ Delay Time	t_{RWS}	—	125	—	100	—	85	—	70	ns
R/$\overline{W}$ Hold Time	t_{HRW}	15	—	15	—	15	—	15	—	ns
Address Delay Time	t_{ADS}	—	125	—	100	—	85	—	70	ns
Address Valid to Ø4 High[4]	$t_{A\phi 4}$	100	—	25	—	10	—	0	—	ns
Address Hold Time	t_{HA}	15	—	15	—	15	—	15	—	ns
Read Access Time	t_{ACC}	775	—	340	—	215	—	160	—	ns
Read Data Setup Time	t_{DSU}	100	—	60	—	40	—	30	—	ns
Read Data Hold Time	t_{HR}	10	—	10	—	10	—	10	—	ns
Write Data Delay Time[2]	t_{WDS}	—	200	—	110	—	85	—	55	ns
Write Data Delay Time[4]	t_{DOW}	—	200	—	110	—	85	—	65	ns
Write Data Delay Time[6]	t_{DD12}	—	450	—	235	—	170	—	120	ns
Write Data Hold Time	t_{HW}	30	—	30	—	30	—	30	—	ns
CONTROL LINE TIMING										
SYNC Delay	t_{SYS}	—	125	—	100	—	85	—	70	ns
RDY Setup Time	t_{RDS}	200	—	110	—	80	—	60	—	ns
$\overline{SO}$ Setup Time	t_{SOS}	75	—	50	—	40	—	30	—	ns
ML Delay Time[5]	t_{MLS}	—	125	—	100	—	85	—	70	ns
ML Hold Time[4]	t_{HML}	10	—	10	—	10	—	10	—	ns
ML Hold Time[6]	t_{HML}	10	—	10	—	10	—	10	—	ns
BE Delay Time[5][8]	t_{BE}	—	40	—	40	—	40	—	40	ns
$\overline{IRQ}$, $\overline{RES}$ Setup Time	t_{IS}	200	—	110	—	80	—	60	—	ns
$\overline{NMI}$ Setup Time	t_{NMI}	300	—	200	—	170	—	150	—	ns

Notes:
1. R65C02 and R65C102 minimum operating frequency is limited by Ø2 low pulse width. All processors can be stopped with Ø2 held high.
2. R65C02 only.
3. Note 3 deleted.
4. R65C102 only.
5. R65C102 and R65C112 only.
6. R65C112 only.
7. Measurement points shown are 0.8V (low) and 2.0V (high) for outputs and 1.5V (low and high) for inputs, unless otherwise specified.
8. BE signal is asynchronous.

This Material Copyrighted By Its Respective Manufacturer



NOTES:
1. R65C02
2. R65C112

Figure 3. Timing Diagram for the R65C02 and R65C112

This Material Copyrighted By Its Respective Manufacturer

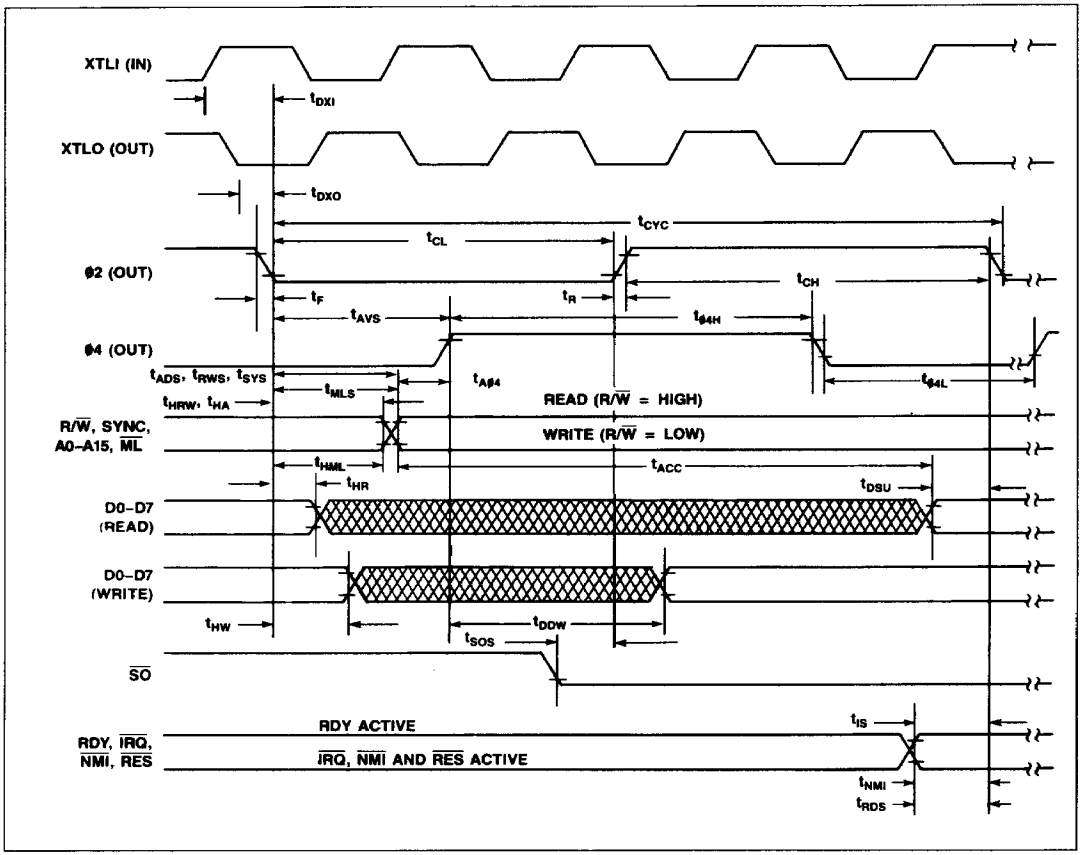
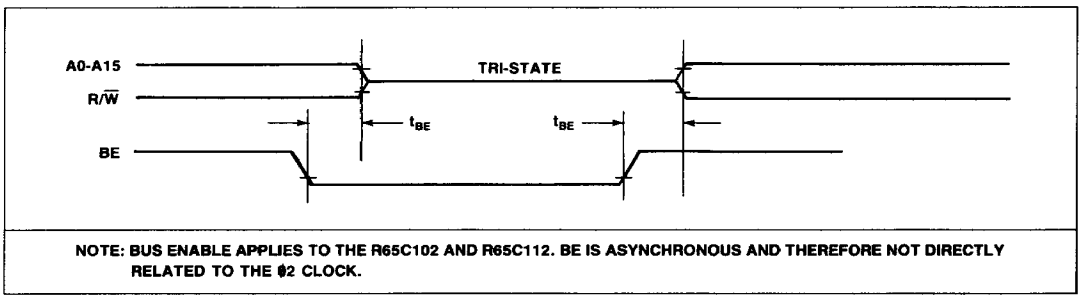


Figure 4. Timing Diagram for the R65C102



NOTE: BUS ENABLE APPLIES TO THE R65C102 AND R65C112. BE IS ASYNCHRONOUS AND THEREFORE NOT DIRECTLY RELATED TO THE Φ2 CLOCK.

Figure 5. Timing Diagram for Bus Enable (BE)

This Material Copyrighted By Its Respective Manufacturer

CLOCK/CRYSTAL CONSIDERATIONS

A crystal controlled time base generator circuit should be used to drive Ø0 (IN) (R65C02) or the XTLI and XTLO (R65C102) inputs. Alternatively, a TTL level clock input to XTLI may be used, with XTLO floating.

Figure 6 shows a time base generation scheme, for a 4 MHz operation of the R65C02, that has been tested and proven reliable for normal environments.

Figure 7 shows a possible external clock scheme for a R65C102 and R65C112 master/slave configuration.

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 7.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 5) = 2C_L \quad \text{or} \quad C = 2C_L - 5$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz, C and C_L is in pF, and R is in ohms.

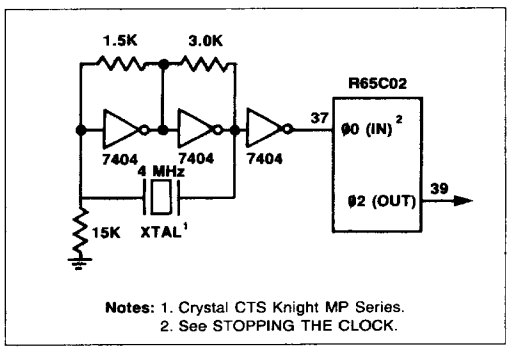
To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 30 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 30) - 5 = 55 \text{ pF}$$
(use standard value of 56 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(4 \times 30)^2} = 138 \text{ ohms}$$

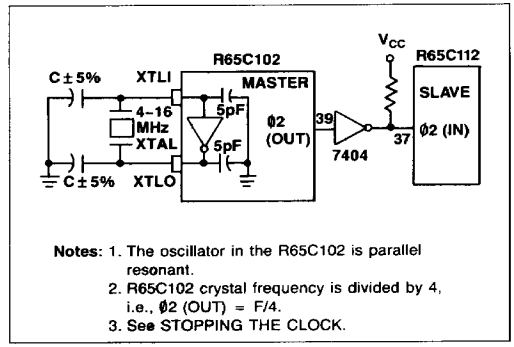


Notes: 1. Crystal CTS Knight MP Series.
2. See STOPPING THE CLOCK.

Figure 6. Example of R65C02 External Time Base Generator Circuit

NOTE

As with any clock oscilltor circuit, stray capacitance due to board layout can affect circuit operation requiring "fine tuning" (e.g. component repositioning or value change) of the circuits shown in Figures 6 and 7. Shunt capacitance (C) includes stray capacitance.

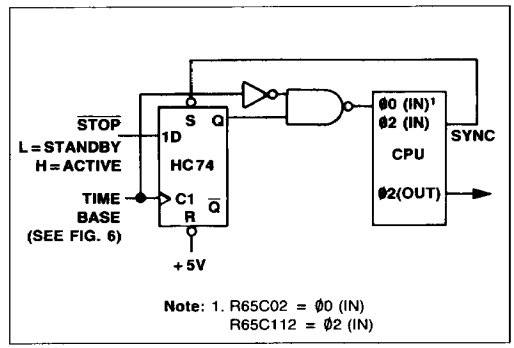


Notes: 1. The oscillator in the R65C102 is parallel resonant.
2. R65C102 crystal frequency is divided by 4, i.e., Ø2 (OUT) = F/4.
3. See STOPPING THE CLOCK.

Figure 7. Example of R65C102/R65C112 Master/Slave Clock Circuit

STOPPING THE CLOCK-STANDBY MODE

Caution must be exercised when configuring the R65C02 or R65C112 in the standby mode (i.e., Ø0 IN or Ø2 IN clock stopped). The input clock can be held in the high state indefinitely; however, if the input clock is held in the low state longer than 5 microseconds, internal register and data status can be lost. Figure 8 shows a circuit that will stop the Ø0 IN (R65C02) or Ø2 IN (R65C112) clock in the high state during standby mode.



Note: 1. R65C02 = Ø0 (IN)
R65C112 = Ø2 (IN)

Figure 8. Stopping the Clock (Standby Mode) Circuit

This Material Copyrighted By Its Respective Manufacturer

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5 Vdc ±5%
Operating Temperature (Ambient) Commercial Industrial Military	T_L to T_H	 0°C to 70°C −40°C to +85°C −55°C to +125°C

ELECTRICAL CHARACTERISTICS

(Over operating conditions unless otherwise noted)

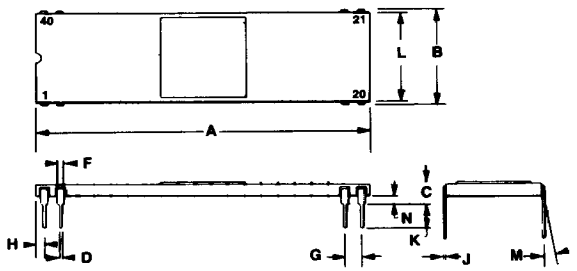
Parameter	Symbol	Min	Typ[4]	Max	Unit	Test Conditions
Input High Voltage −40°C to 85°C −55°C to 125°C	V_{IH}	 2.0 2.4		 V_{CC} +0.3 V_{CC} +0.3	V	
Input Low Voltage −40°C to 85°C −55°C to 125°C	V_{IL}	 −0.3 −0.3		 +0.8 +0.4	V	
Input High Voltage Ø0 R65C02)	V_{IH0}	2.4		V_{CC} +0.3	V	
Input Low Voltage Ø0 (R65C02)	V_{IL0}	−0.3		+0.4	V	
Input High Voltage Ø2 (IN) (R65C112)	V_{IH2}	V_{CC} −0.4		V_{CC} +0.3	V	
Input Low Voltage Ø2 (IN) (R65C112)	V_{IL2}	−0.3		+0.4	V	
Input Leakage Current NMI, IRQ, BE, RDY, RES, SO Ø2 (IN), Ø0 (IN), XTLI	I_{IN}	 — —		 −50 1.0	µA	V_{IN} = 0V to 5.25V V_{CC} = 0V
Three-State (Off State) Input Current Data Lines	I_{TSI}	 —		 10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage SYNC, Data, A0–A15, R/W, Ø1 (OUT), Ø2 (OUT), Ø4 (OUT), ML	V_{OH}	2.4		—	V	V_{CC} = 4.75V I_{LOAD} = −100 µA
Output Low Voltage SYNC, Data, A0–A15, R/W, Ø1 (OUT), Ø2 (OUT), Ø4 (OUT), ML	V_{OL}	 —		+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Supply Current Standby[4] Active (R65C02) Active (R65C102) Active (R65C112) Low Power (R65C02) Low Power (R65C102) Low Power (R65C112)	I_{CC}	 — — — — — — —	 2 2.6 5 2 1.5 3 0.7	 10 4 7 4 2 5 1	 µA mA/MHz mA/MHz mA/MHz mA/MHz mA/MHz mA/MHz	V_{CC} = 5.0V RDY = 0 RDY = 0 RDY = 0
Capacitance NMI, IRQ, SO, BE, RDY SYNC, Data, A0–A15, R/W, Ø1 (OUT), Ø2 (OUT), Ø4 (OUT), ML, XTLO Ø0 (IN), XTLI Ø2 (IN)	 C_{IN} C_{OUT} C_0 C_2	 — — — —		 7 10 10 30	pF	V_{CC} = 5.0V V_{IN} = 0V V_{IN} = 0V f = 1 MHz T_A = 25°C

Notes:
1. All units are direct current (dc).
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. IRQ and NMI require external pull-up resistor.
4. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.

This Material Copyrighted By Its Respective Manufacturer

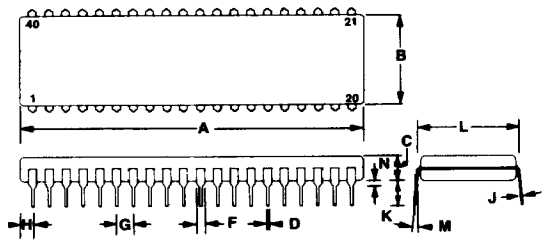
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



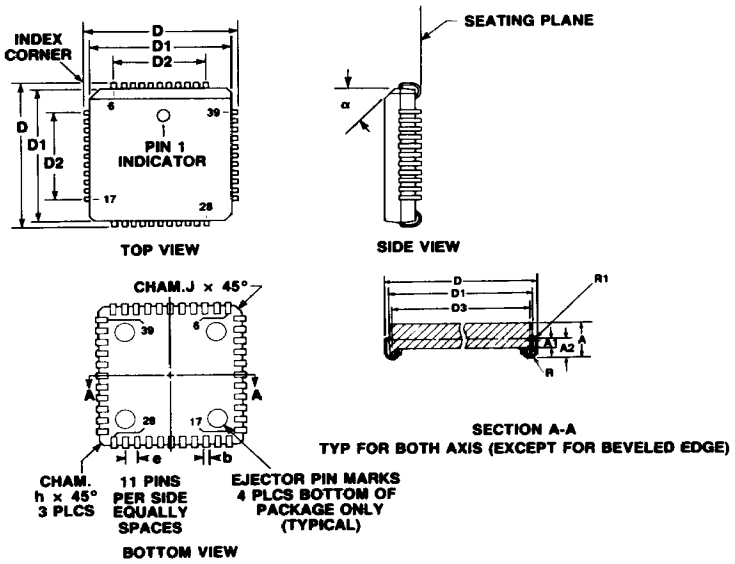
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	15.11	15.88	0.595	0.625
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.27	0.030	0.050
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

This Material Copyrighted By Its Respective Manufacturer